I claim:

1. A CPU system, comprising:

a plurality of CPUs;

a common memory provided for said plurality of CPUs;

an address bus for addressing said common memory;

at least one of said CPUs being connected to said address bus; and

other ones of said CPUs accessing said common memory via said at least one of said CPUs connected to said address bus.

2. The CPU system according to claim 1, including:

a data bus connected to at least one of said CPUs; and

said common memory outputting, via said data bus, data read from said common memory.

3. The CPU system according to claim 1, including:

a data bus connected to at least one of said CPUs; and

said data bus supplying data to said common memory for being written into said common memory.

4. The CPU system according to claim 1, including:

a data read bus connected to said common memory for outputting data read from said common memory;

a data write bus connected said common memory for supplying data to be written into said common memory;

said plurality of CPUs including a given subset of CPUs not connected to said address bus; and

at least some CPUs of said given subset of CPUs being connected to at least one bus selected from the group consisting of said data read bus and said data write bus.

5. The CPU system according to claim 1, including:

a switching apparatus operatively connected to said common memory;

an address memory device operatively connected to said switching apparatus; and

said switching apparatus selectively supplying data output to said address bus by said at least one of said CPUs connected to said address bus and data stored in said address memory device to said common memory as an address.

6. The CPU system according to claim 5, wherein:

said switching apparatus is a multiplexer having a first input connection, a second input connection, and an output connection;

said first input connection is connected, via said address bus, to said at least one of said CPUs connected to said address bus;

said second input connection is connected to said address memory device; and

said output connection is connected to said common memory.

7. The CPU system according to claim 5, wherein said switching apparatus is controlled by said at least one of said CPUs connected to said address bus.

8. The CPU system according to claim 5, wherein:

said address memory device is connected to said address bus and stores addresses; and

said at least one of said CPUs connected to said address bus outputs the addresses stored in said address memory device to said address bus.

9. The CPU system according to claim 5, wherein:

said plurality of CPUs includes given CPUs not connected to said address bus; and

said address memory device has a content, said given CPUs not connected to said address bus being configured to increment the content of said address memory device.

10. The CPU system according to claim 1, wherein:

said plurality of CPUs includes given CPUs not connected to said address bus; and

said given CPUs not connected to said address bus prompt said common memory to perform an operation selected from the group consisting of reading data from said common memory and writing data to said common memory.

11. The CPU system according to claim 10, including:

a memory connectable to said given CPUs not connected to said address bus;

said given CPUs not connected to said address bus outputting addresses for addressing said memory; and

said common memory being configured such that a given signal prompts said common memory to perform an operation selected from the group consisting of reading data from said common memory and writing data to said common memory, the given signal having a profile depending on the addresses output by said CPUs not connected to said address bus.

12. The CPU system according to claim 10, wherein said common memory is configured such that a given signal prompts said common memory to perform an operation selected from the group consisting of reading data from said common memory and writing data to said common memory, the given signal results from a logic combination of specific signals originating from given ones of said plurality of CPUs having a capability of prompting an operation selected from the group consisting of reading data from said common memory and writing data to said common memory, and the specific signals indicating, for each individual one of said plurality of CPUs, whether said

individual one of said CPUs wishes to prompt an operation selected from the group consisting of reading data from said common memory and writing data to said common memory.

13. The CPU system according to claim 10, wherein said common memory is configured such that a given signal prompts said common memory to perform an operation selected from the group consisting of reading data from said common memory and writing data to said common memory, the given signal results from a logic combination of specific signals originating from devices associated with given ones of said plurality of CPUs having a capability of prompting an operation selected from the group consisting of reading data from said common memory and writing data to said common memory, and the specific signals indicating, for each individual one of said plurality of CPUs, whether said individual one of said CPUs wishes to prompt an operation selected from the group consisting of reading data from said common memory and writing data to said common memory.

14. The CPU system according to claim 10, including:

an address memory device operatively connected to said switching apparatus, said address memory device having a memory content;

said common memory is configured such that a given signal prompts said common memory to perform an operation selected from the group consisting of reading data from said common memory and writing data to said common memory; and

said address memory device is configured such that the given signal also prompts said address memory device to increment the memory content.

15. The CPU system according to claim 1, wherein one of said other ones of said CPUs not connected to said address bus transmits data indicating to a relevant one of said plurality of CPUs a start address for an operation selected from the group consisting of reading data from said common memory and writing data to said common memory, when one of said plurality of CPUs, which is to be used for an access and is connected to said address bus, accesses said common memory.

16. The CPU system according to claim 1, wherein one of said other ones of said CPUs not connected to said address bus transmits an address indicating to a relevant one of said plurality of CPUs a start for an operation selected from the group consisting of reading data from said common memory and writing data to said common memory, when one of said plurality of CPUs, which is to be used for an access and is connected to said address bus, accesses said common memory.

17. The CPU system according to claim 15, including:

a switching apparatus operatively connected to said common memory;

an address memory device operatively connected to said switching apparatus;

a given one of said plurality of CPUs, which is used for the operation selected from the group consisting of reading data from said common memory and writing data to said common memory, outputting, to said address bus, the start address indicating a start for the operation selected from the group consisting of reading data from said common memory and writing data to said common memory;

said given one of said plurality of CPUs, which is used for the operation selected from the group consisting of reading data from said common memory and writing data to said common memory, driving said switching apparatus such that data stored in said address memory device are supplied to said common memory as an address; and

said given one of said plurality of CPUs, which is used for the operation selected from the group consisting of reading

data from said common memory and writing data to said common memory, notifying a specific one of said plurality of CPUs, which requested access to said common memory, that said specific one of said plurality of CPUs is allowed to perform an operation selected from the group consisting of reading data from said common memory and writing data to said common memory.

18. The CPU system according to claim 1, wherein said other ones of said CPUs output signals, the signals representing addresses and being used as control signals for controlling system components.

19. The CPU system according to claim 1, wherein said other ones of said CPUs output signals, the signals representing addresses and being converted into control signals for controlling system components.

20. The CPU system according to claim 5, including:

a data bus connected to said address memory device;

said common memory outputting data read therefrom via said data bus; and

said address memory device outputting a content stored therein to said data bus when prompted by one of said CPUs.

21. The CPU system according to claim 20, wherein said address memory device is configured such that a signal for prompting said address memory device to output the content stored therein to said data bus has a signal profile dependent on addresses output by given ones of said CPUs, which are not connected to said address bus, for addressing memories connectable thereto.

22. A CPU system, comprising:

a plurality of CPUs including a first subset of CPUs and a second subset of CPUs;

a common memory provided for said plurality of CPUs;

an address bus for addressing said common memory;

only said first subset of said CPUs being connected to said address bus; and

said second subset of CPUs accessing said common memory via said first subset of CPUs.